Claims

[c1] A method for forming a deep trench capacitor structure, the method comprising the steps of:
(a) forming a deep trench in a semiconductor substrate, said deep trench having an upper region and a lower region;
(b) forming a collar on interior walls of said upper region of said deep trench;
(c) forming a layer of hemispherical silicon grain on exposed interior walls of said lower region of said deep trench;
(d) annealing said substrate in an environment comprising oxygen while simultaneously forming a doped region in said substrate, thereby oxidizing said layer of hemispherical silicon grain and oxidizing a portion of said substrate to form a roughened surface on interior walls of said deep trench; and
(e) removing said oxidized layer of hemispherical silicon grain and said oxidized portion of said substrate.

[c2] The method of Claim 1, wherein said deep trench has a depth and a width, and said depth exceeds said width by at least twenty-five times.

[c3] The method of Claim 1, wherein said semiconductor substrate comprises silicon.

[c4] The method of Claim 3, wherein said semiconductor substrate further comprises a pad oxide film on an upper surface of said substrate and a pad nitride film on said pad oxide film.

[c5] The method of Claim 1, wherein said deep trench is formed using lithography and etching processes.

[c6] The method of Claim 1, wherein said collar comprises oxide and is deposited using tetraethylorthosilicate.

[c7] The method of Claim 1, wherein said collar comprises oxide and is thermally grown.

[c8] The method of Claim 1, wherein said collar comprises nitride.

[c9] The method of Claim 1, further comprising, prior to step (c), the step of subjecting said lower region of said deep trench to an isotropic etching process.

[c10] The method Claim 1, wherein said layer of hemispherical silicon grain is a discontinuous layer having gaps therein which expose portions of said interior walls of said lower region of said deep trench.

[c11] The method of Claim 1, wherein step (d) comprises the steps of:
forming a layer of doped material on said layer of hemispherical silicon grain and on exposed interior walls of said deep trench; and
annealing said substrate in an environment comprising oxygen.

[c12] The method of Claim 1, wherein step (d) comprises the step of:
annealing said substrate in an environment comprising oxygen and at least one dopant species.

[c13] The method of Claim 1, wherein said oxidized layer of hemispherical grain silicon and said oxidized layer portion of said substrate are removed using an oxide etchant comprising HF.

[c14] The method of Claim 1, further comprising the step of removing said collar simultaneously with said removal of said oxidized layer of hemispherical silicon grain and said oxidized portion of said substrate

[c15] The method of Claim 1, after step (e), further comprising the steps of:
(f) forming a node dielectric layer on interior walls of said deep trench; and

(g) filling said deep trench with a conducting material.

[c16] The method of Claim 15, wherein said node dielectric layer comprises silicon nitride, and said conducting material comprises arsenic-doped polysilicon.

[c17] A method for forming a deep trench capacitor structure, the method comprising the steps of:
forming a deep trench in a semiconductor substrate, said deep trench having an upper region and a lower region;
forming a collar on interior walls of said upper region of said deep trench;
forming a layer of hemispherical silicon grain on exposed interior walls of said lower region of said deep trench;
forming a layer of arsenic-doped material on said layer of hemispherical silicon grain and on exposed interior walls of said lower region of said deep trench;
annealing said substrate in an environment comprising oxygen, thereby simultaneously forming a doped region in said substrate, oxidizing said layer of hemispherical silicon grain and oxidizing a portion of said substrate to form a roughened surface on interior walls of said lower region of said deep trench; and
removing said oxidized layer of hemispherical silicon grain and said oxidized portion of said substrate.

[c18] The method of Claim 17, further comprising, prior to forming said layer of hemispherical silicon grain, the step of subjecting said lower region of said deep trench to an isotropic etching process.

[c19] The method Claim 17, wherein said layer of hemispherical silicon grain is a discontinuous layer having gaps therein which expose portions of said interior walls of said lower region of said deep trench.

[c20] The method of Claim 17, further comprising the step of removing said collar simultaneously with said removal of said oxidized layer of hemispherical silicon grain and said oxidized portion of said substrate.

[c21] A method for forming a deep trench capacitor structure, the method comprising the steps of:
forming a deep trench in a semiconductor substrate, said deep trench having an upper region and a lower region;
forming a collar on interior walls of said upper region of said deep trench;
forming a layer of hemispherical silicon grain on exposed interior walls of said lower region of said deep trench;
annealing said substrate in an environment comprising oxygen and at least one dopant species, thereby simultaneously forming a doped region in said substrate, oxi-

dizing said layer of hemispherical silicon grain and oxidizing a portion of said substrate to form a roughened surface on interior walls of said lower region of said deep trench; and
removing said oxidized layer of hemispherical silicon grain and said oxidized portion of said substrate.

[c22] The method of Claim 21, further comprising, prior to forming said layer of hemispherical silicon grain, the step of subjecting said lower region of said deep trench to an isotropic etching process.

[c23] The method Claim 21, wherein said layer of hemispherical silicon grain is a discontinuous layer having gaps therein which expose portions of said interior walls of said lower region of said deep trench.

[c24] The method of Claim 21, further comprising the step of removing said collar simultaneously with said removal of said oxidized layer of hemispherical silicon grain and said oxidized portion of said substrate.